CLAIMS

What is claimed is:

1. A clock synthesizer for deriving at least one output clock signal from a source clock signal, comprising:

a phase generator configured to generate a first predetermined number of phases of the source clock signal, the phases of the source clock signal defining a plurality of phase sectors;

a phase selector configured to select respective pairs of the phases of the source clock signal, each selected pair of phases bounding a respective one of the phase sectors; and

a phase interpolator configured to introduce at least one phase of the source clock signal between each pair of phases to provide a second predetermined number of phases of the source clock signal within each phase sector, the phase interpolator being further configured to successively output the phases of the source clock signal to derive the output clock signal having a stepped up or stepped down frequency.

2. The clock synthesizer of claim 1,

wherein the phase generator is configured to generate a predetermined number P of phases of the source clock signal, the P phases of the source clock signal defining P phase sectors, and

wherein the phase interpolator is configured to introduce at least one phase of the source clock signal between each pair of phases to provide a predetermined

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number Q of phases of the source clock signal within each phase sector,

the phase interpolator being further configured to successively output the phases of the source clock signal to produce lagging or leading phase shifts of about 360/P(Q-1) degrees to derive the output clock signal having the stepped up or stepped down frequency.

3. The clock synthesizer of claim 2 wherein the predetermined number P of phases of the source clock signal is greater than or equal to 4.

4. The clock synthesizer of claim 1 wherein the phase generator is configured to generate the first predetermined number of evenly spaced phases of the source clock signal.

5. The clock synthesizer of claim 1 wherein the phase interpolator is configured to introduce at least one phase of the source clock signal between each pair of phases to provide the second predetermined number of evenly spaced phases of the source clock signal within each phase sector.

6. The clock synthesizer of claim 1 further including control circuitry configured to control the phase selector and the phase interpolator, the control circuitry including a state machine having a plurality of states, the phase interpolator being configured to successively output the phases of the source clock signal based on the plurality of states.

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7. The clock synthesizer of claim 6 wherein the plurality of states comprises a plurality of ordered states, and the control circuitry is configured to transition through the states in a forward or reverse order to derive the output clock signal.

8. The clock synthesizer of claim 6 wherein each state corresponds to a respective combination of sector codes and thermometer codes, each sector code corresponding to a respective one of the phase sectors, each thermometer code corresponding to a weight that each one of the first predetermined number of phases of the source clock signal contributes to the derivation of the output clock signal.

9. The clock synthesizer of claim 1 wherein the phase generator is configured to generate the first predetermined number of phases of the source clock signal from a high frequency signal that is at least two times a desired frequency of the source clock signal.

10. The clock synthesizer of claim 1 wherein the phase interpolator comprises a differential interpolator.

11. The clock synthesizer of claim 1 wherein the phase generator is selected from the group consisting of a ring oscillator and a coupled LC oscillator.

12. A method of operating a clock synthesizer to derive at least one output clock signal from a source clock signal, comprising the steps of:

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generating a first predetermined number of phases of the source clock signal by a phase generator, the phases of the source clock signal defining a plurality of phase sectors;

selecting respective pairs of the phases of the source clock signal by a phase selector, each selected pair of phases bounding a respective one of the phase sectors;

introducing at least one phase of the source clock signal between each pair of phases to provide a second predetermined number of phases of the source clock signal within each phase sector by a phase interpolator; and

successively outputting the phases of the source clock signal to derive the output clock signal having a stepped up or stepped down frequency by the phase interpolator.

13. The method of claim 12,

wherein the generating step includes generating a predetermined number P of phases of the source clock signal, the P phases of the source clock signal defining P phase sectors,

wherein the introducing step includes introducing at least one phase of the source clock signal between each pair of phases to provide a predetermined number Q of phases of the source clock signal within each phase sector, and

wherein the outputting step includes successively output the phases of the source clock signal to produce lagging or leading phase shifts of about 360/P(Q-1)

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degrees to derive the output clock signal having the stepped up or stepped down frequency.

14. The method of claim 13 wherein the predetermined number P of phases of the source clock signal is greater than or equal to 4.

15. The method of claim 12 wherein the generating step includes generating the first predetermined number of evenly spaced phases of the source clock signal.

16. The method of claim 12 wherein the introducing step includes introducing at least one phase of the source clock signal between each pair of phases to provide the second predetermined number of evenly spaced phases of the source clock signal within each phase sector.

17. The method of claim 12 further including the step of controlling the phase selector and the phase interpolator by control circuitry, the control circuitry including a state machine having a plurality of states, and wherein the outputting step includes successively outputting the phases of the source clock signal based on the plurality of states.

18. The method of claim 17 wherein the plurality of states comprises a plurality of ordered states, and wherein the controlling step includes transitioning through the states in a forward or reverse order to derive the output clock signal.

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19. The method of claim 17 wherein each state corresponds to a respective combination of sector codes and thermometer codes, each sector code corresponding to a respective one of the phase sectors, each thermometer code corresponding to a weight that each one of the first predetermined number of phases of the source clock signal contributes to the derivation of the output clock signal.

20. The method of claim 12 wherein the generating step includes generating the first predetermined number of phases of the source clock signal from a high frequency signal that is at least two times a desired frequency of the source clock signal.

21. The method of claim 12 wherein the phase interpolator comprises a differential interpolator.

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